

DESIGN AND PERFORMANCE EVALUATION REPORT

November 1, 1967

Prepared Under

Contract NAS5-10539
Magnetic Tape Link Optimization Study

For

National Aeronautics & Space Administration Goddard Space Flight Center Greenbelt, Maryland 20771

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By

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TABLE OF CONTENTS

Ι

TECHNICAL MEMORANDUM G-103-1

"Design Report: Magnetic Tape Link Optimization Study"

Section		Page
1	OBJECTIVE	1
2	PERFORMANCE ANALYSIS	2
	2.1 Tape Response	2 7 11
3	TAPE SIMULATOR	15
4	SYNCHRONIZATION TECHNIQUES	17
5	BIT DETECTION	22
	5.1 Theory of Operation	22 23
6	TEST PROCEDURES	26
	6.1 Test Equipment	26 31
	II	
"Perí	TECHNICAL MEMORANDUM G-103-2 formance Evaluation Report: Magnetic Tape Link Optimization S	Study''
Section		<u>Page</u>
1	INTRODUCTION	35
2	EXPERIMENTAL MEASUREMENTS	36
	2.1 Pulse Response Tests	36 40 41
3	PERFORMANCE CALCULATIONS	41
4	DISCUSSION AND CONCLUSIONS	40



LIST OF ILLUSTRATIONS

I

TECHNICAL MEMORANDUM G-103-1

"Design Report: Magnetic Tape Link Optimization Study"

Figure		Page	
1	Recording Technique	3	
$\overline{2}$	Idealized Tape Link Amplitude Response	4	
3	Output Waveform, $1/T = f_r$	5	
4	Peak Signal and Intersymbol Interference as a		
	Function of Bit Rate	6	
5	Error Probabilities in the Presence of	Ť	
	Intersymbol Interference	9	
6	Error Propability as a Function of E/N_0	12	
7	Tape Recorder Amplitude Responses	·14	
8	Tape Simulator	16	
9	Tape Output, Two Consecutive Identical Bits $(1/f_rT) = 1$.	18	
10	Tape Output, Two Consecutive Dissimilar Bits $(1/f_rT) = 1$.	19	
11	Synchronization	20	
12	Zero Crossing Recovery Unit	21	
13	Timing Diagram Zero Crossing Recovery Unit	22	
14	Bit Detection	24	
15	Timing Diagram	25	
16	Test Equipment Configuration Using Synchronization	-	
	Method #1	27	
17	Test Equipment Configuration Using Synchronization		
	Method #2	28	
18	Binary Data Format	29	
	II		
			
"Perfo	TECHNICAL MEMORANDUM G-103-2 ormance Evaluation Report: Magnetic Tape Link Optimization St	udy''	
<u>Figure</u>		Page	
1a	Pulse Response Test Waveforms (Input Waveform)	36	
. 1b	Pulse Response Test Waveforms (Output Waveform)	37	
2	Unequalized Output Waveforms for Various Bit Durations .	38	
3	Equalized Output Waveforms for Various Bit Durations	39	
4	Unequalized Tape Recorder Amplitude Response 42		
5	Error Probability as a Function of S/σ		
6	Error Performance of Proposed Scheme, Compared		
	with Conventional Recording	47	



TECHNICAL MEMORANDUM G-103-1

REFERENCE: Contract No. NAS 5-10539

FROM: C. Boardman, R. Chufo

DATE: 3 August 1967

SUBJECT: Design Report: Magnetic Tape Link Optimization Study

1. OBJECTIVE

In an earlier study,* we reported on the advantages of recording splitphase binary data using an un-equalized magnetic tape recorder. The advantage
of this method of processing is the ability to achieve high tape packing density.
This arises from the fact that the tape recorder forms approximately a matched
filter for the split-phase waveform. This design report describes the experimental study which we will undertake to confirm the conclusions of the earlier
theoretical study. The specific objectives of this study are:

- a) To experimentally determine the error performance of the proposed recording method for various packing densities.
- b) To demonstrate that it is feasible to extract bit synchronization from a split-phase data sequence which has been recorded in the recommended manner.
- c) To compare the performance obtained with the performance of conventional techniques for split-phase recording.**

In this design report we first present some analytic results which supplement earlier performance studies of the proposed recording technique. In Sec. 3 we discuss the design of the tape link simulator to be constructed and used in Task II. In Sec. 4 we present two methods of synchronization. Both methods will be implemented in Task II and tested in Task III. In Sec. 5 we present the

^{*}See Final Report, NASA Contract NAS5-9705, Task XI.

Data on conventional recording of split-phase data will not be obtained in this program; it must be supplied by GSFC.



design of bit detection circuitry which will be built during Task II and used in Task III. Finally, in Sec. 6 we present a plan for the tests to be performed during Task III.

2. PERFORMANCE ANALYSIS

Earlier performance analysis of the proposed recording technique was restricted to one particular bit-packing density determined by the tape characteristic. In this report we extend the analysis to include a suitable range of bit rates such as we plan to use in the experimental study. With higher bit rates, intersymbol interference becomes significant in degrading data quality. We take this into account in calculating error probabilities for the system. This extension will permit more comparison between experimental data and theoretical prediction.

2.1 Tape Response

The proposed processing scheme is shown schematically in Fig. 1. The split-phase input waveform is considerably distorted in passing through the tape recorder. The resulting waveform is sampled at the instant of its peak; the polarity of this sample determines which binary output is produced by the signal detection equipment.

According to the model which we assumed, the transfer function of the un-equalized tape recorder is

$$H(j\omega) = \sqrt{e} j \frac{\omega}{\omega_{r}} e^{-\frac{1}{2}(\omega/\omega_{r})^{2}} e^{-j\omega t} o$$
 (1)

The frequency $\omega_r = 2\pi f_r$ determines the location of the peak in the amplitude response (see Fig. 2). The step response corresponding to Eq. 1 is

$$\sqrt{\frac{e}{2\pi}} e^{-\frac{1}{2}\omega_{r}^{2}(t-t_{o})^{2}}$$
 (2)

The split-phase (baseband) waveform is

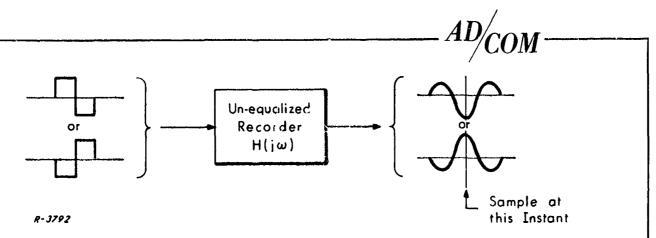


Fig. 1 Recording Technique

$$x(t) = \sqrt{\frac{E}{T}} \left[u \left(t + \frac{T}{2} \right) - 2u(t) + u \left(t - \frac{T}{2} \right) \right]$$
 (3)

The bit period is T sec and the amplitude is chosen so that the energy per bit is E. This scaling is for convenience in calculation only; in actual recording input levels are chosen to give maximum output without saturation. From Eqs. 2 and 3, the response of the tape link is found to be

$$y(t) = \sqrt{\frac{e}{2\pi} \left(\frac{E}{T}\right)} \left[e^{-\frac{1}{2}\omega_{r}^{2} \left(t+T/2-t_{o}\right)^{2} - 2 e^{-\frac{1}{2}\omega_{r}^{2} \left(t-t_{o}\right)^{2} + e^{-\frac{1}{2}\omega_{r}^{2} \left(t-T/2-t_{o}\right)^{2}} \right]$$
(4)

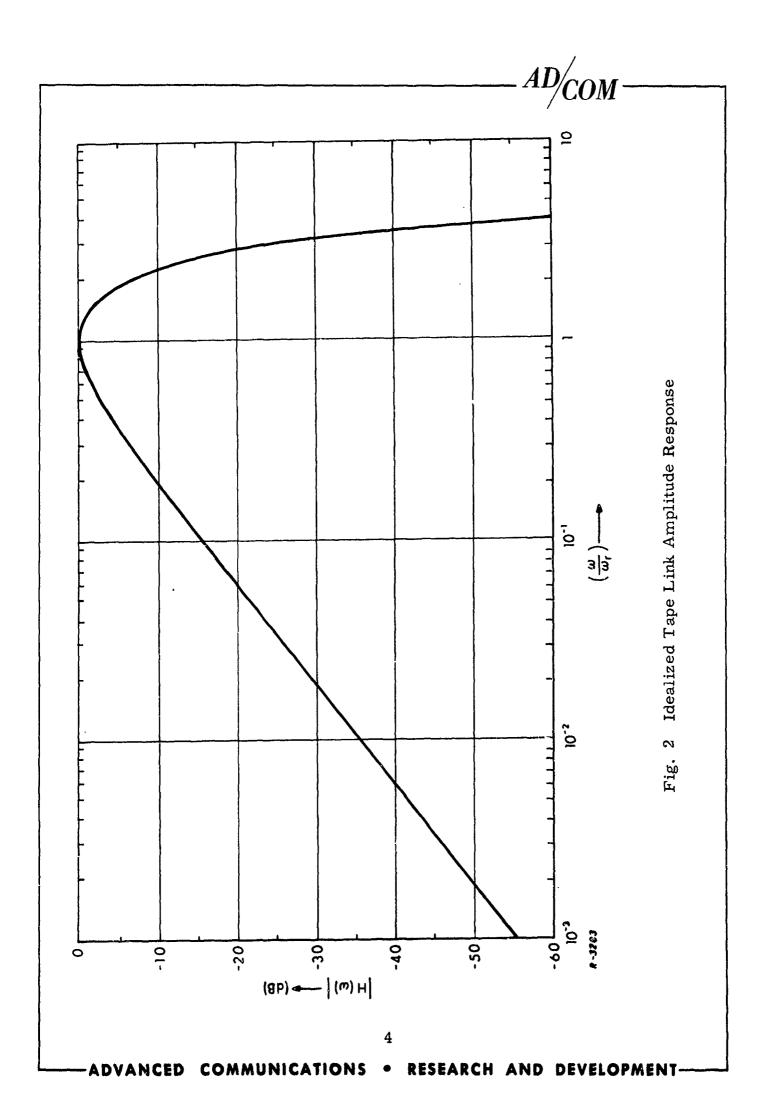
So far, we have not assumed any relationship between the bit rate 1/T and the characteristic frequency of the tape response, f_r . To plot Eq. 4 (Fig. 3) we have chosen 1/T equal to f_r . This will illustrate features which appear for other bit rates as well.

It is clear from Fig. 3 as well as from Eq. 4 that the peak of the output waveform occurs at $t = t_0$. The magnitude of this peak is found by replacing the argument of Eq. 4 by t_0 , giving

$$y(t_o) = -2\sqrt{\frac{e}{2\pi}(\frac{E}{T})} \left[1 - e^{-\frac{1}{2}(\omega_r T/2)^2} \right]$$
 (5)

This is plotted as a function of bit rate in Fig. 4. Its magnitude falls off gradually for bit rates greater than f_r .

Another property of interest is intersymbol interference. For the case we have plotted in Fig. 3 the magnitude of the response at $t - t_0 = \pm T$ (corresponding to the sampling instants of the adjacent bits) is negligible. This is not





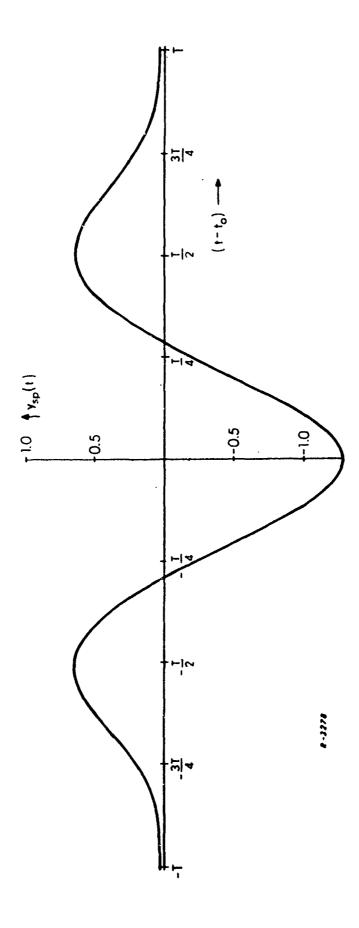
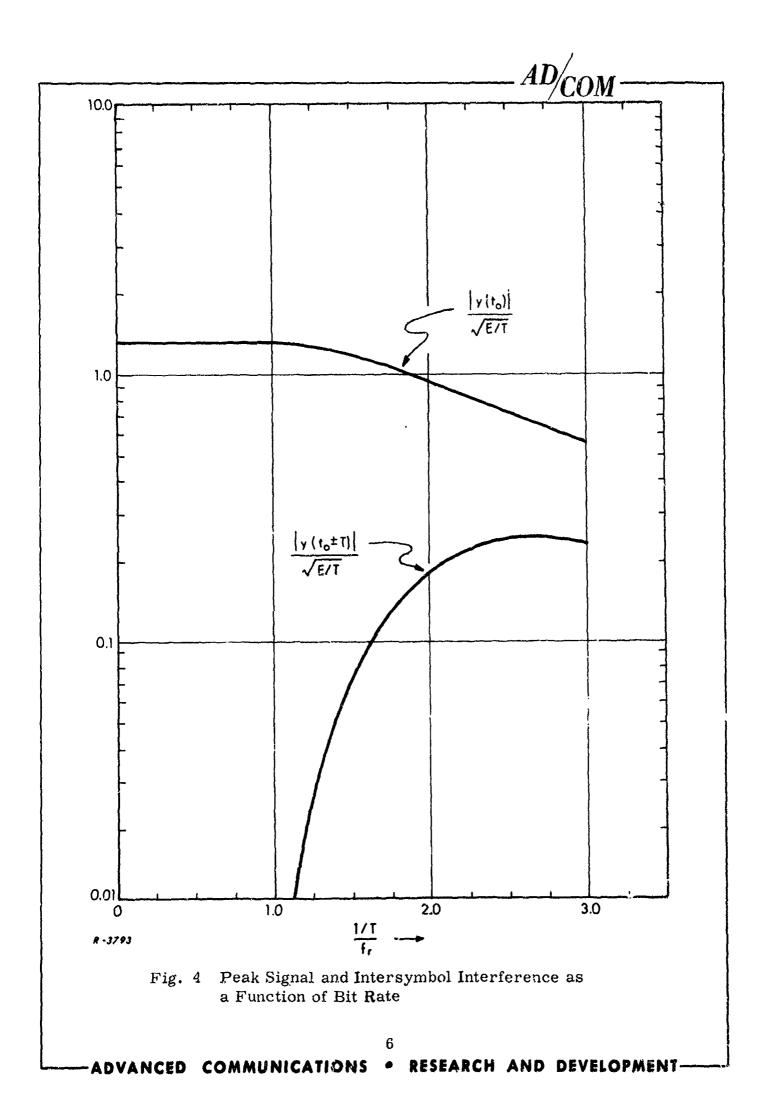


Fig. 3 Output Waveform, $\frac{1}{\Gamma} = f_r$



the case as the bit rate is increased. Substituting $t_0 \pm T$ for the argument of Eq. 4 we find

$$y(t_{o} \pm T) = \sqrt{\frac{e}{2\pi} \left(\frac{E}{T}\right)} \left[e^{-\frac{1}{2} \left(\omega_{r} T/2\right)^{2}} - 2 e^{-2 \left(\omega_{r} T/2\right)^{2}} + e^{-\frac{9}{2} \left(\omega_{r} T/2\right)^{2}} \right]$$
(6)

This is also plotted in Fig. 4 as a function of bit rate. Intersymbol interference increases abruptly as bit rate is increased and becomes significant for bit rates more than 1-1/2 times the characteristic frequency f_r . Because of this rapid increase, intersymbol interference is a more important cause of data degradation than the decrease of signal amplitude which also occurs for higher bit rates. In the next section we will determine this degradation quantitatively.

2.2 Average Err r Performance

The decision process which takes place at the output of the recorder in Fig. 1 is a simple and well-known one. The waveform is sampled at a particular instant of time and a decision is made, based on the sign of the sample. If the possible signal amplitudes (corresponding to the binary "1" and "0") are +S and -S at the sampling instant and the additive Gaussian noise has variance σ^2 , it is well known that the probability of error is

$$P_{e} = 1 - \Phi(\frac{S}{\sigma}) \tag{7}$$

The function $\Phi(x)$ is the Gaussian distribution function defined by

$$\Phi(x) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{x} e^{-y^2/2} dy$$
 (8)

When intersymbol interference is present it takes the form of an additional signal voltage not related to the bit being detected, and this result must be modified.



In the present problem, each pulse interferes equally with the two pulses immediately preceding and succeeding it. This is due to the symmetry of the pulse shape (Fig. 3). If the intersymbol interference caused by one pulse has amplitude I, then the total intersymbol interference may assume the three values -2I, 0, or +2I. The conditions under which these values occur are explained by Table 1 which shows all combinations of polarities of the three pulses (assuming for convenience that the pulse being detected has positive polarity). In the first case the interference from both adjacent pulses adds to the signal amplitude; in the second case the interference voltages from the adjacent pulses are of opposite polarity, so they cancel each other; and so on. It is clear that in the first case the error probability (Eq. 7) is given by

$$1 - \Phi\left(\frac{S + 2I}{\sigma}\right) ; \tag{9}$$

in the second case it is given by

$$1 - \Phi\left(\frac{S}{\sigma}\right)$$
; (10)

and so on. If the data is random and uncorrelated from bit-to-bit, each of the four cases occurs with probability one-fourth, so we may write the complete error probability as

$$P_{e} = \frac{1}{4} \left\{ \left[1 - \Phi\left(\frac{S + 2I}{\sigma}\right) \right] + \left[1 - \Phi\left(\frac{S}{\sigma}\right) \right] + \left[1 - \Phi\left(\frac{S}{\sigma}\right) + \left[1 - \Phi\left(\frac{S - 2I}{\sigma}\right) \right] \right\}$$

$$= 1 - \frac{1}{4} \left[\Phi\left(\frac{S + 2I}{\sigma}\right) + 2\Phi\left(\frac{S}{\sigma}\right) + \Phi\left(\frac{S - 2I}{\sigma}\right) \right]$$
(11)

This result is plotted in Fig. 5 for several values of the interference-to-signal ratio I/S. It is clear that the effect of intersymbol interference is negligible when I/S is less than 0.1. However, values of I/S much larger than this produce substantial data degradation.

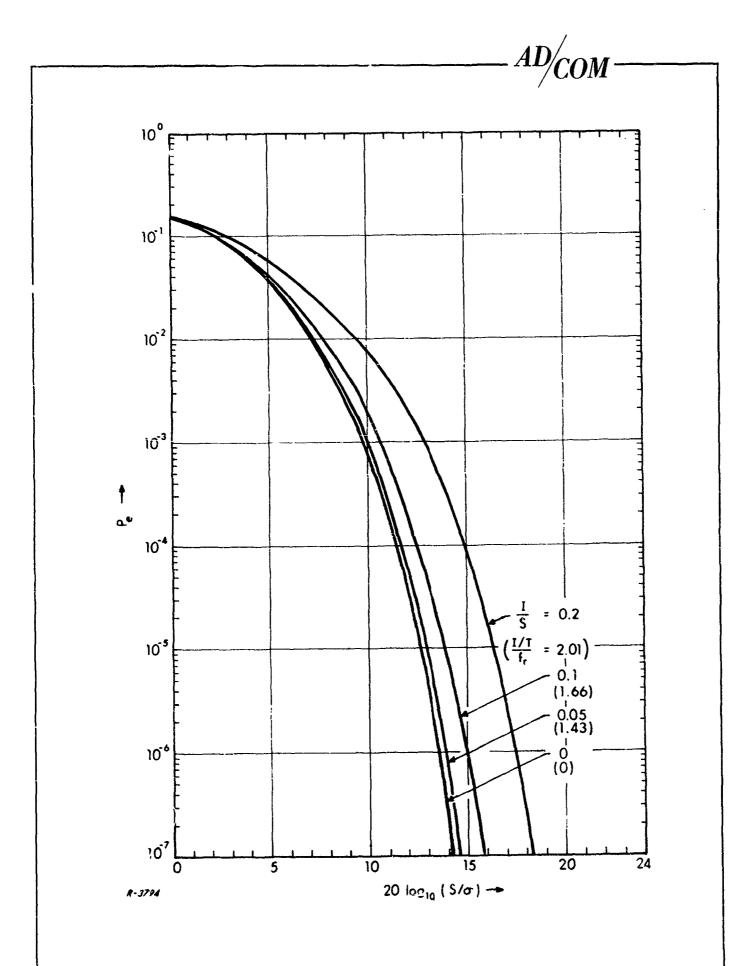


Fig. 5 Error Probabilities in the Presence of Intersymbol Interference

TABLE 1

Possible Polarities of a Sequence of Pulses and Resulting Signal Amplitudes

Polarity of Preceding Pulse	Polarity of Pulse Being Detected	Polarity of Following Pulse	Total Signal Present
+	+	+	S + 2I
+	+	-	S
-	+	+	s
-	+	-	S - 2I

From Fig. 4 we may determine what bit rates produce a given I/S ratio. Accordingly the curves of Fig. 5 are also labeled with the corresponding bit rate. In terms of bit rate, intersymbol interference becomes significant at a bit rate equal to about 1-2/3 the roll-off frequency f_r and causes substantial degradation for bit rates greater than twice the roll-off frequency.

It is more convenient to have error curves plotted as a function of signal energy-to-noise density ratio E/N_o , than in terms of S/σ . The conversion is accomplished by finding the output voltage in terms of signal energy E (and the bit period T) from Eq. 5 or Fig. 4. Output noise power σ^2 is found in terms of input noise density N_o from the relationship

$$\sigma^2 = \frac{N_o}{2} \int_{-\infty}^{\infty} |H(j\omega)|^2 d\omega \qquad (12)$$

where $H(j\omega)$ is the tape transfer function given by Eq. (1). Integration of Eq. (12) gives

$$\sigma^2 = 1.204 \text{ N}_{0} \text{ r}$$
 (13)

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Combining these two results we obtain the conversion relationship

$$\frac{S}{\sigma} = 3.00 \frac{1 - e^{-\frac{1}{2} \left(\frac{\omega_r T}{2}\right)^2}}{\sqrt{\omega_r T}} \sqrt{\frac{E}{N_o}}$$
(14)

Using this conversion Eq. (11) has been replotted as a function of E/N_{C} for various values of bit rate in Fig. 6. The values of relative bit rate $\left(\frac{1}{T}/f_{r}\right)$ have been chosen as convenient integers. These will be the values used in the experimental phase of this program. For comparison the optimum performance urve is also plotted. This result is given by the formula

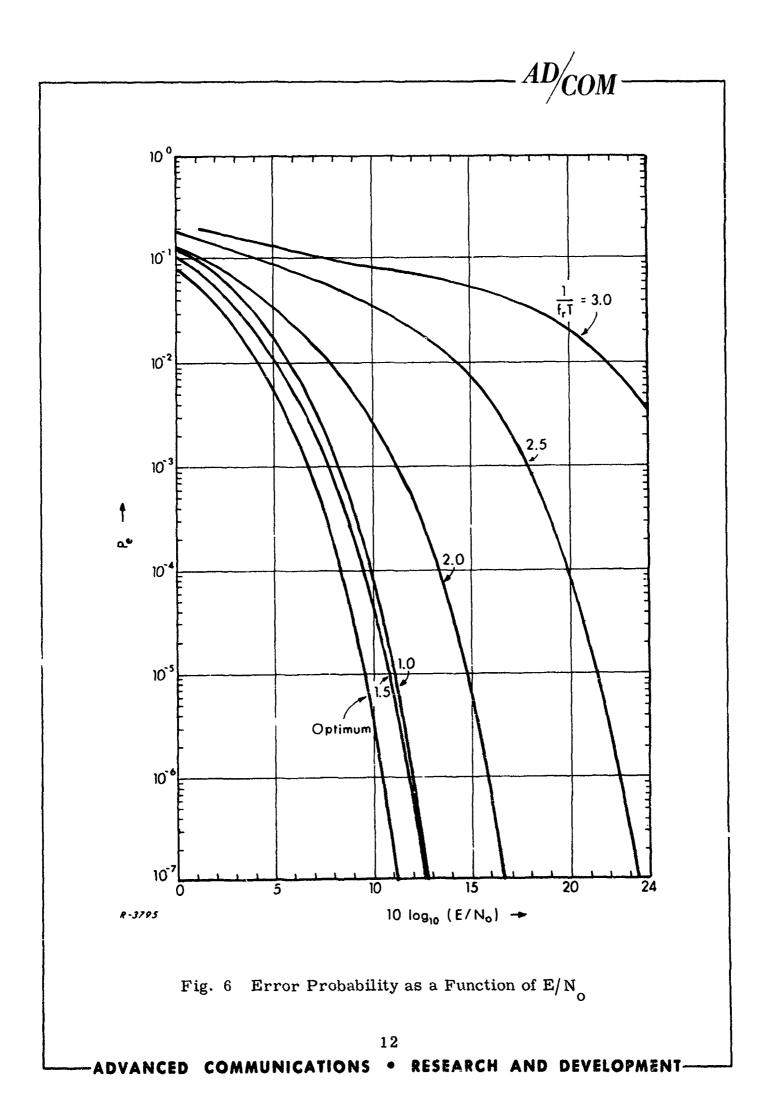
$$P_{e} = 1 - \Phi \left(\sqrt{\frac{2E}{N_{o}}} \right) \tag{15}$$

The curves for $1/f_rT = 1$ and $1/f_rT = 1-1/2$ are both close to the optimum. For higher bit rates performance is worse. This is due to both intersymbol interference and the fact that for higher bit rates the tape head characteristic no longer approximates a matched filter for the split-phase waveform. The fact that the $1/f_rT = 1$ curve shows worse performance than $1/f_rT = 1-1/2$ is because the head characteristic is better matched to the higher bit rate. This overcomes the small loss in performance due to increased intersymbol interference.

The analysis up to this point has been in terms of relative bit rate $(1/f_rT)$. In the next section we relate this to actual bit rate by determining the nominal roll-off frequency f_r characteristic of the tape head response of the Ampex FR-600 tape recorder.

2.3 Nominal Tape Characteristic

The tape response model of Fig. 2 is normalized to the roll-off frequency f_r . This parameter completely describes any actual tape characteristic which



conform to the model. In order to design the equipment which will be used in this test program it was necessary to know the bit rates which will be used. The bit rates chosen will, of course, depend on the parameter f_r of the tape wavelink to be used. Since the tape recorder was not available during Task I, its response could not be measured directly. Therefore f_r was estimated from manufacturers specifications.

The available manufacturer's literature does not include information about tape head response alone; therefore it was impossible to estimate f directly. However, by combining a graph of equalizer amplitude response and the overall amplitude response specifications, it is possible to deduce the head characteristic. The tape speed selected was 60 ips. The corresponding equalizer response is reproduced from the Ampex manual in Fig. 7. The overall response specification for this speed is

± 3 db from 300 to 250,000 Hz

A possible response curve meeting this specification is shown in Fig. 7. This curve is not unique, of course, many other curves could be drawn within this specification. However, it is a good approximation to the true curve. The head characteristic may be found by subtracting the equalizer response from the overall response; this has been done to obtain the curve shown on Fig. 7. This curve has its maximum at $f_r = 47 \text{ kHz}$.

The value of f_r we have obtained is subject to two kinds of error. First of all, we assumed an overall response curve which may not be the correct one. Second, all of the information we used is indicative of the response of a "typical" tape recorder. In the experimental phase (Task III) we will be working with a particular recorder which may or may not be "typical". For these reasons, the value of f_r we have obtained must be considered an approximate one, for design purposes only. When the actual recorder is available (Task III), we will measure its amplitude response in order to obtain an accurate value of f_r for that

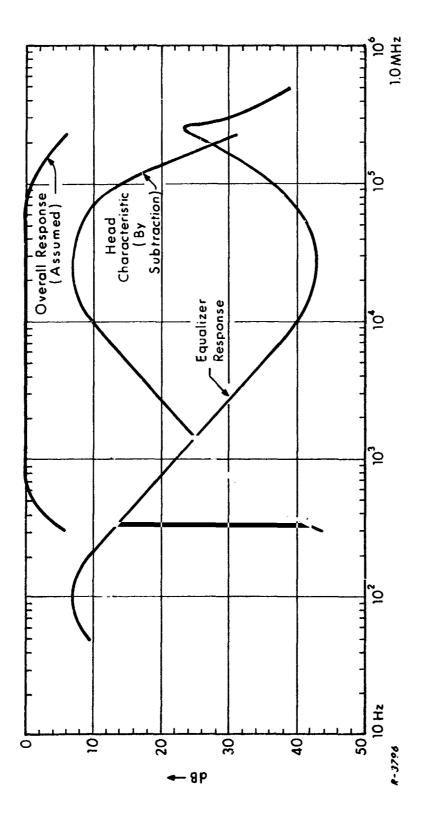


Fig. 7 Tape Recorder Amplitude Responses



particular recorder. With all of this understood, it is interesting to look at the bit rates and bit packing densities to be used in the experimental program.

Table 2 lists relative bit rate, actual bit rate, and bit packing density for the values to be tested.

TABLE 2

Bit Rates and Bit Packing Densities
(Assuming f_r = 47 kHz)

Relative Bit Rate	True Bit Rate 1/T	Packing Density 1 T × 60 ips
1	47 k bits/sec	0.78 k bits/inch
1 -1/2	71	1.18
2	94	1.57
2-1/2	118	1.96
3	141	2. 35

3. TAPE SIMULATOR

Task II of the program consists of building all necessary test equipment (including modifications of existing equipment) and performing preliminary tests prior to more thorough testing at GSFC. The primary objective of these tests will be to determine if the synchronization and bit detection circuitry are operating as desired. To do this it is necessary to have a data stream such as would be produced at the output of an un-equalized tape recorder. Since the FR-600 tape machine will not be available at ADCOM for these preliminary tests, a simple tape simulator will be constructed. This simulator will be a linear filter with transfer function approximately that of the tape head model (Fig. 2).

The roll-off frequency of the simulator will be 47 kHz, as determined from Fig. 7. The fact that this nominal characteristic may not be identical with the actual tape recorder used in Task III is of no consequence. Tests made in this task will be at bit rates appropriate to the simulator. This will be sufficient to determine if the synchronizer and bit detector are operating properly. In Task III bit rates will be chosen to correspond to the actual tape characteristic. Both the synchronizer and bit detector will be flexible enough, with regard to data rate, to accept any change that may result.

The simplest way of simulating the unequalized tape response is with a differentiator and low-pass filter in series. A circuit to accomplish this is shown in Fig. 8. The cut-off frequency of the R-C differentiator is chosen for good linearity in the region below the cut-off frequency of the low-pass filter. This is done by placing the cut-off frequency of the R-C combination at 94 kHz (twice the cut-off frequency of the low-pass filter). The transmission loss at 47 kHz will then be 7 db. A laboratory variable low-pass filter follows the differentiator and provides a roll-off of 18 db/octave (SKL Model 300).

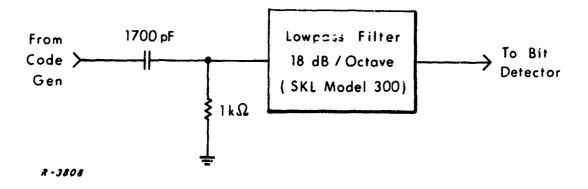


Fig. 8 Tape Simulator

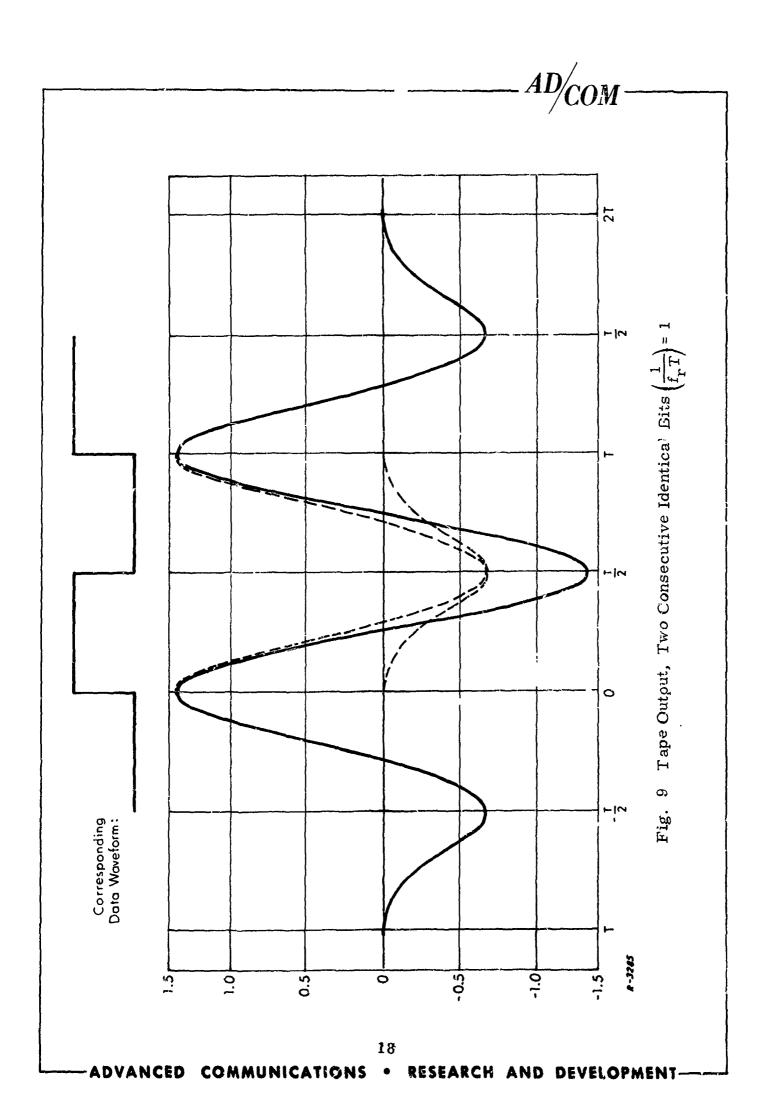
4. SYNCHRONIZATION TECHNIQUES

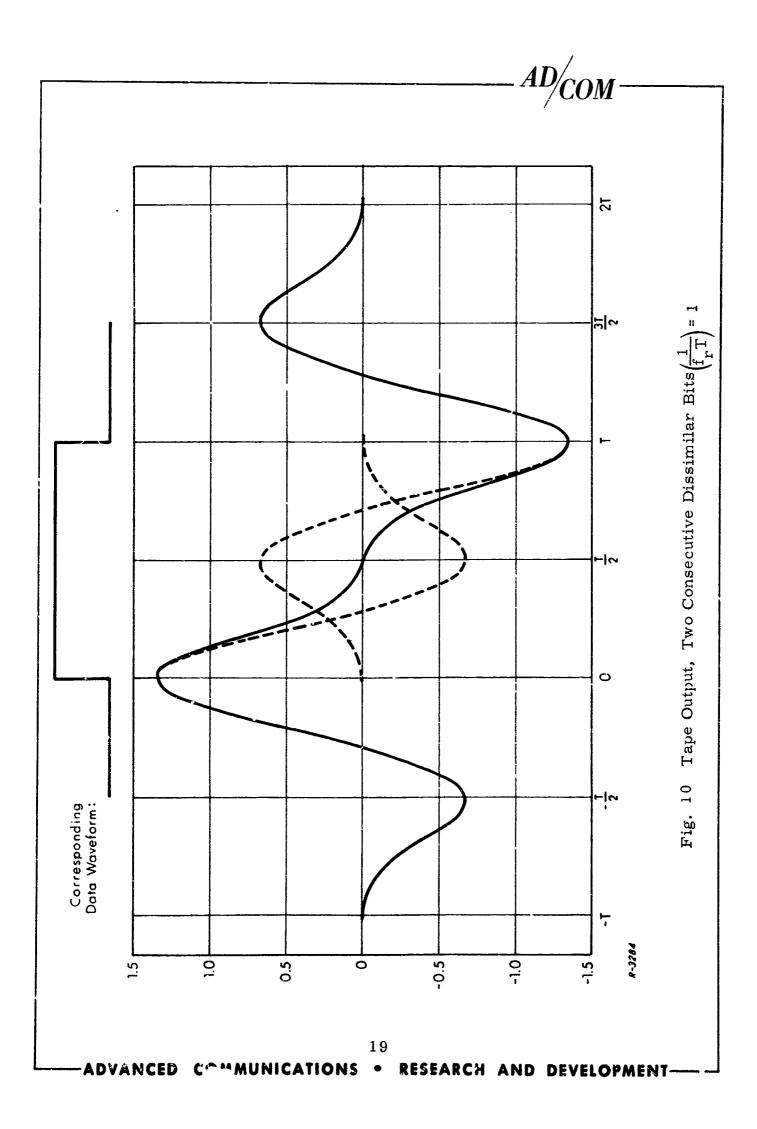
In this section we describe two methods of deriving clock synchronization. The first method utilizes the existing equalizer to derive a split-phase waveform from the read head output. The second method requires building a zero crossing recovery unit. Both methods make partial use of the unmodified Model 305 PCM Bit Synchronizer to regenerate the clock and perform logic functions.

The necessity for developing unusual synchronization methods arises from the distortion of the SP waveform recorded in an unequalized tape recorder. This is illustrated (for the case $1/f_{\rm r}T=1$) by Fig. 3. In Figs. 9 and 10 we have plotted the output produced by two consecutive bits of similar (Fig. 9) or dissimilar (Fig. 10) polarity. Examination of these shows that the periodic zero crossing at the center of the bit period and the intermittent zero crossing between bits are no longer present. These zero crossings are normally used by signal conditioners such as the Monitor 305 to establish synchronization. The two methods described below have been developed to operate in spite of the absence of these zero crossings.

Fig. 11 is the block diagram of the synchronizer. In the first method, the reproduce amplifier (and equalizer) is switched into the circuit and provides an undistorted split-phase output to the input of the signal conditioner. This is possible because the equalized bandwidth of the FR-600 (250 kHz at 60 ips) is considerably greater than most of the bit rates to be used. This method of synchronization will be marginal at the higher bit rates (118 and 141 bits/sec) because the equalized bandwidth will not be great enough to pass the SP waveform without considerable distortion. The bit synchronizer locks onto the double frequency component in the split-phase input and therefore produces a 180° ambiguity in the phase of the clock output.

This ambiguity is resolved by logic circuitry within the bit synchronizer which operates on the basis of the following characteristics of the split phase





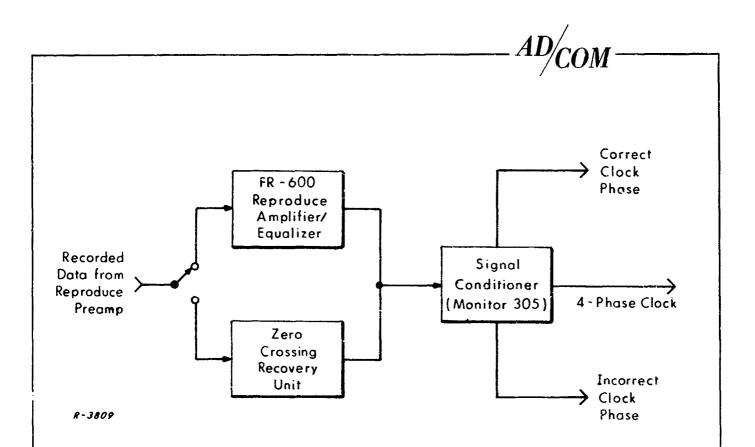


Fig. 11 Synchronization

Lignal. The split-phase signal always has a transition in the middle of a bit. The signal may or may not have a transition at the end of a bit. Therefore the transition density at the middle of bits is greater than at the end of bits. Assuming that the clock is properly phased, the middle of each bit corresponds to a negative transition of the 0° clock, and the end of each bit corresponds to a positive transition of the 0° clock. An up-down counter compares the density of data transitions at the positive clock transitions and compares it with the density of data transitions at negative clock transitions to determine if the clock is properly phased. Logic signals corresponding to norma! (correct) phasing and reversed (incorrect) phasing are available at pins 32 and 4 respectively of the split-phase card assembly. This information will be used to choose which clock zero crossing will control the sample gate in the bit detection unit.

In the second method, the zero crossing recovery unit shown in Fig. 12 is switched into the circuit. This device takes advantage of the fact that every

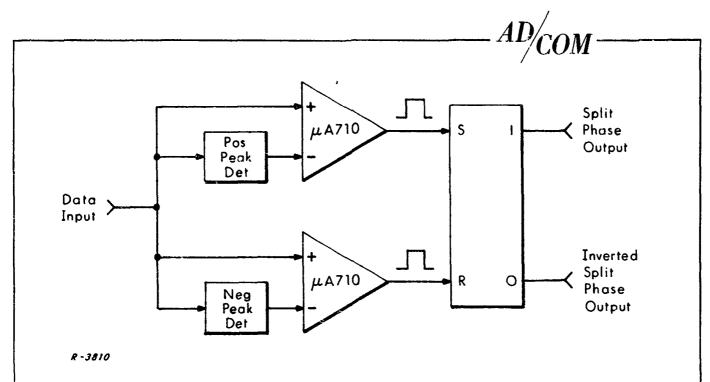
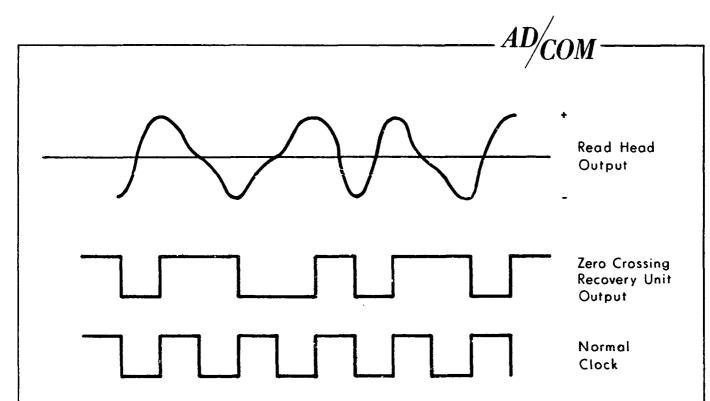


Fig. 12 Zero Crossing Recovery Unit

transition in the original data waveform produces a positive or negative peak in the tape head output. From Figs. 9 and 10 it can be seen that negative transitions in the data produce negative peaks in the output, while positive transitions produce positive peaks. The zero crossing recovery unit regenerates a split-phase waveform by detecting the positive and negative peaks and generating corresponding transition in its output, as shown in Fig. 13. This function can be performed by two voltage comparators and a R-S Flip-Flop as in Fig. 12. The voltage comparators produce positive pulses at present voltage levels and cause the flip-flop to change states when these levels are exceeded. In order to automatically regulate the trigger point of the comparators and thus compensate for varying input signal levels, the data is also fed to positive and negative peak detectors. Part of the peak detector output is then used to reference the comparators so that they will trigger at a given percentage of the peak data level.

The output of the zero-crossing recovery unit is actually a crudely detected replica of the original split-phase waveform. With this as input, the phase-locked loop of the signal conditioner produces an accurate clock waveform which provides timing information to the bit detection unit. The bit detection unit, in turn, produces a more accurate replica of the original split-phase waveform by using near-optimum detection.



R-3811

Fig. 13 Timing Diagram Zero Crossing Recovery Unit

5. BIT DETECTION

5.1 Theory of Operation

In addition to the synchronization operation described in the preceding section, our system must perform the operations of bit detection and data reconstruction. The principal underlying this operation is quite simple. The output of the tape head (via the reproduce preamplifier) must be sampled periodically (at the location of the peak caused by each bit) and the polarity of this sample used to determine the value of the corresponding bit in the reconstructed data waveform. In addition to these operations of sampling and data reconstruction, the bit detection unit described in this section incorporates a variable delay and automatic phase selection controlled by the bit synchronizer.

The necessity for having a variable delay in the bit detection unit arises because the clock output from the signal conditioner will not always be in phase with the data input to the bit detection unit. In synchronization method #1 this phasing error will be introduced by the reproduce amplifier (and equalizer) which

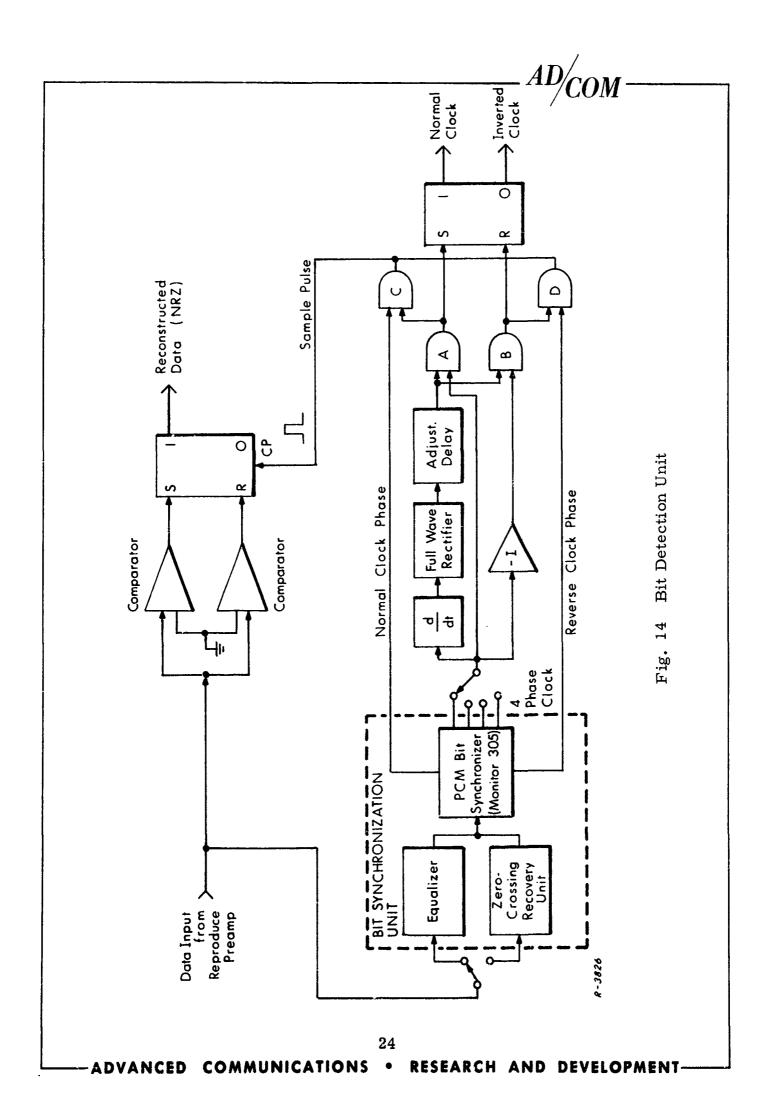
precedes the signal conditioner. In synchronization method #2, phasing error is introduced by the nature of the peak-to-transition conversion process performed by the zero crossing recovery unit. Since peaks are detected at their leading edges, rather than their exact centers, the signal conditioner output will lead the data waveform slightly. The bit detection unit contains an adjustable delay which delays both the clock waveform and the sampling time. Since the signal conditioner provides a 4-phase clock, a clock phase can always be found which is less than 1/4 bit ahead of the data waveform. Therefore the adjustable delay in the bit detection unit must be adjustable only from zero to 1/4 bit. In operation this delay need be adjusted only once for a given bit rate and synchronization method.

The automatic phase reversal feature of the bit detection unit is necessitated by the manner in which the signal conditioner resolves the ambiguity (see Sec. 4) in phase. The phase of the clock output from the signal conditioner is established before the signal conditioner resolves the phase ambiguity and is unchanged by this or any later phasing decision. Therefore the clock waveform may be 180° out of phase from the data waveform. Logic signals indicating normal or reverse phase are taken from the signal conditioner, and control the sampling time of the bit detection unit accordingly. However, the clock output from the bit detection unit is not affected by this phasing information.

5.2 Circuit Operation

A block diagram of the circuit is shown in Fig. 14 and relevant waveforms in Fig. 15. The timing operations take place in the lower half of Fig. 14. One of the clock phases is chosen* by a manual switch. It is differentiated and full-wave rectified to provide timing pulses at the ends and midpoint of each bit (see Fig. 15). These pulses are delayed by an adjustable delay circuit (using monostable multivibrators) to provide trigger pulses for the delayed clock. The pulses are steered into the proper terminals (Set or Reset) of a flip-flop by AND

^{*}When setting up the unit for a particular bit rate.



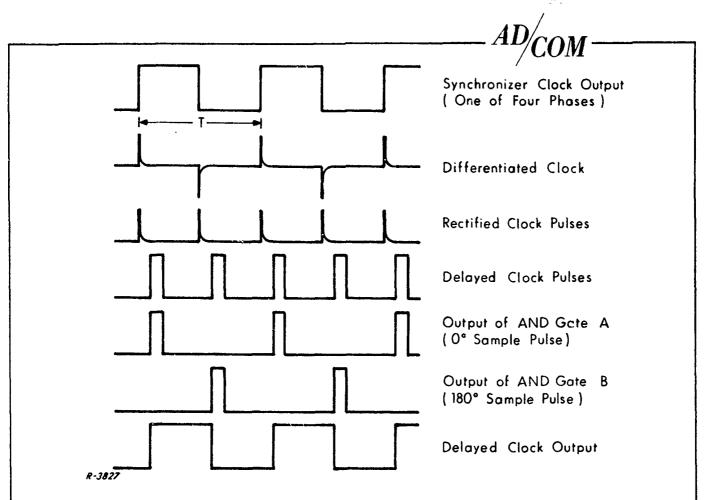


Fig. 15 Timing Diagram

gates A and B. The Set input line has only pulses corresponding to the heading edge of the input pulse (0°), and the Reset input line had the alternate pulses corresponding to the tracking edge of the input pulse (180°). This prevents the output clock from being 180° out of phase with the input, in addition to the desired phase shift. The output of the flip-flop is the desired delayed version of the clock.

One of the two input lines to the flip-flop is selected by AND gates C and D to control the bit detection. If the normal clock phase signal from the signal conditioner is present, AND gate C allows the 0° timing pulses from the Set line to read the detection circuitry at the top of Fig. 14. On the other hand, if the reverse clock phase signal is present, AND gate D allows the 180° timing pulses to control bit detection.

The actual bit detection circuitry consists of two comparators and a gated flip-flop. A signal is produced by the upper comparator if the input signal is positive and by the lower if it is negative. Therefore a signal is present at the Set input of the flip-flop if the input is positive or at the Reset input if it is negative. The timing pulse gates the flip-flop at the beginning of each bit, producing an NRZ-C data stream at the output of the flip-flop. This (together with the clock waveform) is the desired output from the bit detection unit. Note that the reconstructed data and the output clock are in phase with each other, although both have been delayed.

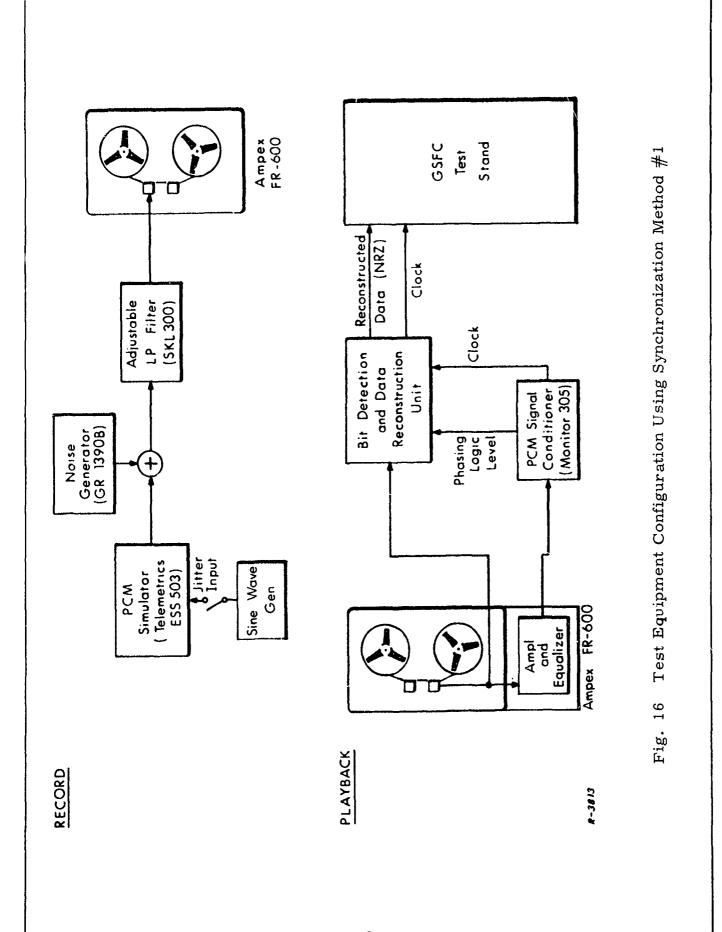
6. TEST PROCEDURES

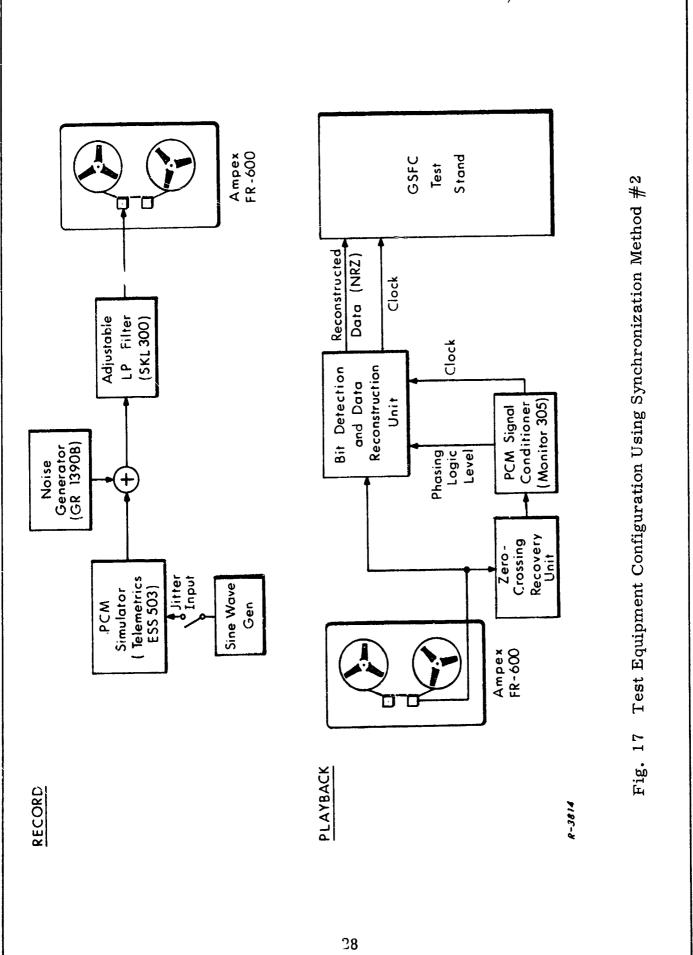
In this section we discuss the test procedures to be used in Task III of the program. First we describe how the equipment will be utilized to make error performance measurements. Then we discuss the choice of parameters, operating conditions, etc., under which performance will actually be measured.

6.1 Test Equipment

The equipment configurations to be used are shown in Figs. 16 and 17. Figure 16 shows the configurations for operation with synchronization method #1; Fig. 17 shows operation with synchronization method #2. Both configurations will be tested to determine the relative advantages of the synchronization methods. In either method recording procedures are identical and are described below.

Referring to Figs. 16 or 17, a Telemetrics Model ESS 503 PCM Simulator will be used to generate an SP data stream. This simulator is fully adjustable in bit rate, so it will be possible to generate all the bit rates listed in Table 2. The simulator has an input for introducing any desired bit rate jitter. The simulator is capable of generating the signal format shown in Fig. 18. All frames are identical. The first part of each frame is a fixed pseudo-random sequence required by the GSFC error-counting equipment. The remainder of the frame may





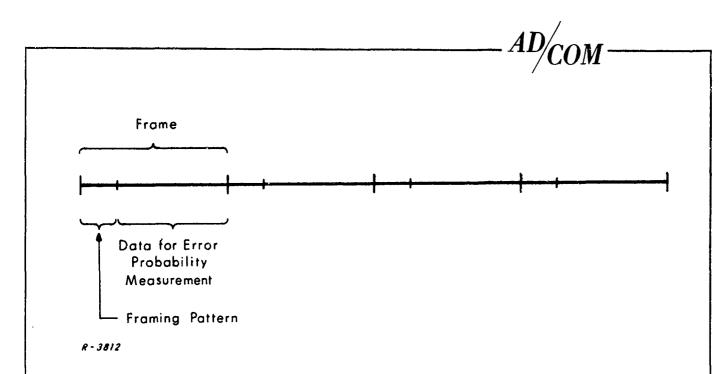


Fig. 18 Binary Data Format

be any desired sequence of SP data. Various sequences will be used (see Sec. 6.2) to test operation of the synchronization and detection units under diverse conditions. No modifications will be required to the PCM simulator in order to perform these functions.

The data stream from the PCM simulator is combined additively with the output of a random noise generator. This generator should produce a noise spectrum which is flat over the spectral region where the data waveform has significant energy. A random split-phase wave-train has significant energy content out to about four times the bit rate. Since the maximum bit rate anticipated is 141 kbits/sec, this means that a noise spectrum of 1/2 MHz width is sufficient. A GR1390-B Random Noise Generator is adequate for this purpose. Both the noise generator and the PCM simulator have output level control which will be used to adjust the energy-to-noise-density ratio E/N_o.

The low-pass filter following the PCM simulator and noise generator serves two purposes. First of all, it can be used in measuring the noise density N_O. With the data signal shut off, the noise generator output is passed through a known bandwidth low-pass filter. The power in this bandwidth can be measured.

with a true rms meter; this establishes the noise density i... The second purpose of the low-pass filter is to limit the harmonic content of the signal waveform. This will be done to simulate actual operating conditions, where the recorder obtains its input from a receiver with band-limited output. However, it is expected that because of the band limiting being performed by the tape recorder, additional band-limiting prior to the tape link will have little effect.

After passing through the low-pass filter, the signal and noise are recorded in the normal manner. After recording a convenient length of tape, it is replayed at some later time. The reproduce amplifier (including equalization) of the FR-600 is used only in synchronization method #1. Otherwise, tape output is obtained directly from the reproduce preamplifier which precedes the reproduce amplifier.

Operation of the synchronization and detection units which recover the can from the tape output has been described fully in Secs. 4 and 5 of this memorandum. In synchronization method #1, the tape recorder equalization is used to restore the zero crossing to the distorted output of the tape recorder before it is fed to the Monitor 305 conditioner. In method #2 the Zero Crossing Recovery Unit generates a waveform with zero crossings at the appropriate instants. In either case the signal conditioner (Monitor 305) operates in its normal manner without any internal modifications. Its output is four phases of clock waveform. However, a phasing ambiguity results from the fact that the phase locked loop internal to the signal conditioner is operating at twice the bit rate. The signal conditioner resolves this ambiguity internally, but does not correct the clock output. Therefore, because the proposed detection method performs bit detection external to the signal conditioner, it is necessary to extract a logic signal from the signal conditioner to indicate which phase of the clock output is correct. This logic level together with the four clock phases is used by the bit detection unit in determining when to sample the data waveform from the tape preamplifier.

The output of the bit detection unit is a replica of the original data stream in NRZ-C format, and the four-phase clock. These are supplied to GSFC test equipment which determines the average error probability for the tape segment.

6.2 Tests to be Performed

In the preceding section we described how a length of tape is recorded and played back. The result of this operation is a value of average error rate. In order to obtain curves of error probability (such as those in Fig. 6) it is necessary to repeat the operation a number of times. Each repetition involves a segment of tape recorded at a different value of E/N_0 . The error probabilities obtained from each run can be plotted to form a complete error probability curve. This is the basic form in which data will be taken. In this section we describe the various conditions under which error probability curves will be obtained.

The first objective of the test program is to determine how high a bit rate is practical with this method of recording. Therefore a series of error probability curves will be obtained at the tape speeds shown in Table 2. This series will be repeated with both synchronization methods, to provide a comparison between the two. Since there are five speeds listed in Table 2, this will involve ten complete error probability curves. It is possible that at the higher bit rates synchronization will not be possible. If this is the case, these curves will be omitted. Those tests will be performed with noise as the only degrading factor. In other words, there will be no bit rate jitter, no amplitude jitter, and no limitation of harmonic content of the data waveform. The data format used will be a pseudo-random pattern, so as to duplicate the conditions of the analytic results of Sec. 2.

After the above series of tests has been completed it will be possible to select the bit rates of most interest for more thorough testing. If the analytic results of Fig. 6 are reliable, the lower bit rates have no substantial advantage in error performance over a bit rate such as $1/f_{\rm r}T=2$. The latter is clearly of more interest because of the higher packing density involved. Higher bit rates offer packing advantage at the expense of considerable error performance degradation. With the experimental error curves available, one or two bit rates will be selected which make the best compromise between these two considerations. For this bit rate (or rates, if two are chosen) further error probability curves will be taken under various conditions as described below. Unless one of the synchronization methods has been eliminated in the previous testing, both methods will receive the series of tests described below.

The effect of different data sequences will be investigated by repeating the error probability curves under each of the following conditions.

- 1) Data consisting of all ones, or of all zeros.
- 2) Data consisting of alternating ones and zeros (that is, 1 0 1 0 1 0, etc.)

The effect of bit rate jitter will be studied using a sinusoidal jitter input to the PCM simulator. The use of sinusoidal jitter permits controlled variation of both maximum bit rate deviation and the rate of change of bit rate. Since the Monitor Signal Conditioner is being used without internal modification, it is expected that tolerance to bit rate jitter will be equivalent to the specifications for the Monitor Unit. According to specification, this unit will:

- 1) Acquire synchronization for bit rates within 10%.
- 2) Maintain synchronization for bit rates within 25%.
- 3) Maintains synchronization for bit rate changes up to 1% per second.



These specifications are in the absence of noise, so no noise input will be used. Presence or absence of synchronization will be indicated by the "out of synch" indicator on the signal conditioner and by the observed error probability. If the experimental system fails to meet any of the three specifications above, the corresponding condition will be reduced until the system meets it. This will define new specifications which apply to the system under test.

During the course of Tasks II and III experience with the equipment involved may suggest other tests which will be of interest. Such tests, plus tests suggested by the Technical Officer, will be carried out in Task III.



TECHNICAL MEMORANDUM G-103-2

Reference: Contract No. NAS5-10539

From: C.J. Boardman, A.F. Ghais

Date: 22 September 1967

Subject: Performance Evaluation Report: Magnetic Tape Link

Optimization Study

1. INTRODUCTION

This Technical Memorandum is a sequel to the design report submitted on August 3, 1967 and designated Technical Memorandum G-103-1. Together, they constitute a complete design plan for the experimental evaluation of an unconventional technique for recording and reproducing split-phase PCM signals, as well as a performance evaluation of the technique based on preliminary experimer al measurements.

The design report (G-103-1) contained an analytical evaluation of the performance of the proposed recording/reproducing technique, based on an assumed analytical model of the tape recorder. The result indicated performance inferior to that presently attained by GSFC personnel using conventional techniques. Specifically, for the same data-packing density on tape, the unconventional technique suffered significantly reduced detectability.

These results could not be considered conclusive, however, because the validity of the assumptions underlying the performance calculations could not be determined without laboratory investigation. In order to obtain realistic performance information on which the proper course of further investigation could be based, the cognizant GSFC technical officer requested ADCOM to perform the necessary preliminary experimental measurements and performance calculations.



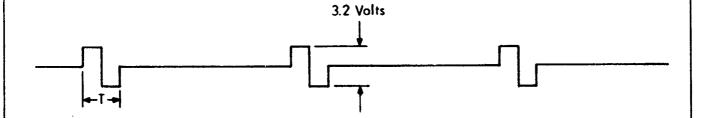
The present memorandum documents those preliminary experiments, the data obtained, and the performance calculations based on them. A discussion of the results follows, and conclusions are drawn.

2. EXPERIMENTAL MEASUREMENTS

The purpose of this section is to record the experimental data obtained at the GSFC facilities. All tests were performed on the Ampex FR-600 tape recorder operated at 15 ips. All gain adjustments in the tape recorder electronics were constant during the series of tests.

2.1 Pulse Response Tests

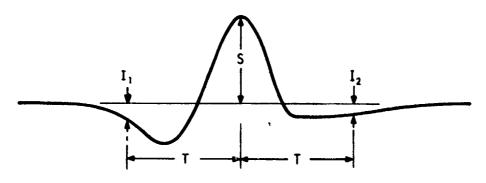
Intersymbol-interference was measured directly by recording the periodic waveform shown in Figure 1a. Each split-phase waveform is followed by an interval with no input signal, to allow measurement of the "tails" of the response. The interval between pulses is much greater than the bit duration T. The tape was reproduced on-line and the (unequalized) output waveform from the reproduce preamplifier was observed on an oscilloscope. The peak voltage, S, was recorded, together with the voltages T sec before and after the peak, as indicated in Figure 1b. These voltages (I₁ and I₂) represent interference with the preceeding and succeeding bits, respectively.



a) Input Waveform

Figure 1. Pulse Response Test Waveforms





b) Output Waveform

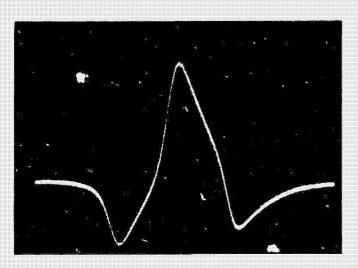
Figure 1. Pulse Response Test Waveforms

The observed values of S, I_1 and I_2 are shown in Table 1, for a range of bit durations. The peak-to-peak input voltage for these tests was 3.2 volts. Oscilloscope photographs of the unequalized output waveforms are shown in Figure 2; for comparison, photographs of the equalized output are shown in Figure 3.

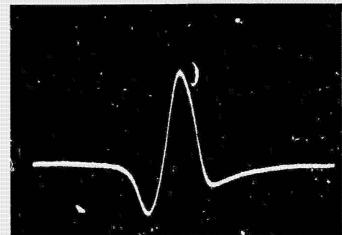
Table 1
PULSE RESPONSE VOLTAGES FOR VARIOUS BIT DURATIONS

T	Equivalent Bit Rate	I ₁ *	S*	I ₂ *
80 μs	12.5 kb/s	1 mv	104 mv	7 mv
40 μs	25 kb/s	12 mv	80 mv	8 mv
26.7 μs	37.5 kb/s	0 mv	64 mv	7 mv
20 µs	50 kb/s	8 mv	44 mv	3 mv
16 µs	62.5 kb/s	9 mv	33 mv	4 mv

^{*} All volt ge readings ±2 mv, due to experimental uncertainties.



a) 12.5 kb/s Vert: 10 mV/cm Hor: 20 μs/cm



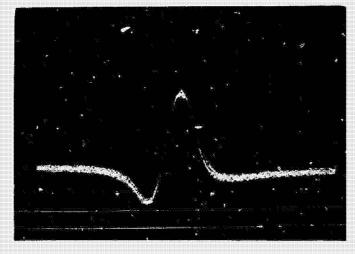
b) 25 kb/s Vert: 10 m⁻/cm Hor: 20 μs/cm



c) 37.5 kb/s Vert: 5mV/cm Hor: 10µs/cm



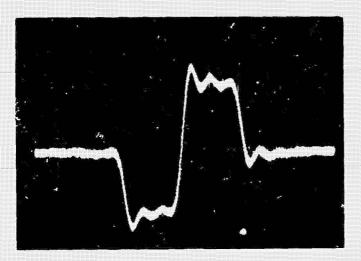
d) 50 kb/s Vert: 5mV/cm Hor: 10µs/cm



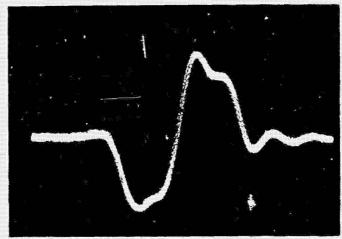
e) 62.5 kb/s Vert: 5 mV/cm Hor: 10 \(\mu\)s/cm

R-3977

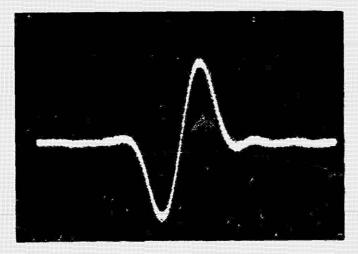
Fig. 2 Unequalized Output Waveforms for Various Bit Durations



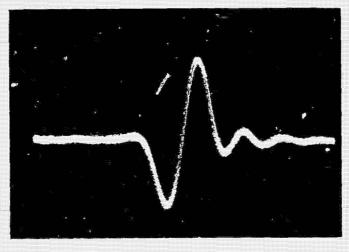
a) 12.5 kb/s Vert: 1 v/cm Hor: 20μs/cm



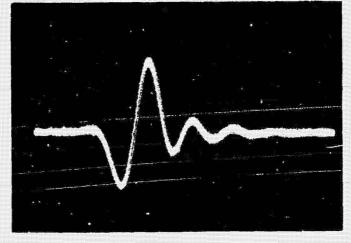
b) 25 kb/s Vert: 1 v/cm Hor: 10μs/cm



c) 37.5 kb/s Vert: 1 v/cm Hor: 10µs/cm



d) 50 kb/s Vert:1 v/cm Hor:10 μs/cm



e) 62.5 kb/s Vert; lv/cm Hor: 10 μs/cm

R-3978

Fig. 3 Equalized Output Waveforms for Various Bit Durations

2.2 Noise Bandwidth

The second test performed was a measurement of the tape recorder noise bandwidth. Input to the recorder was a noise spectrum obtained by passing flat noise through a 20 Hz to 100 kHz bandpass filter.* The output level (v_i) of the bandpass filter (measured with a true rms meter) was 2 volts rms. The rms output voltage (σ) from the recorder under these conditions was 69 mv.

The (un-normalized) noise bandwidth of a device, B, is defined as the ratio between the noise power out and the input noise density; that is,

$$B_n = \frac{\sigma^2/R_0}{N_0} Hz$$
 (1)

where R_o is the load resistance at the output and N_o is the input noise density in watts/Hz. In this experiment σ was measured. N_o is given by the measured input power divided by the bandwidth of the bandpass filter. That is,

$$N_{O} = \frac{v_{i}^{2}/R_{i}}{(100 \times 10^{3} - 20)}$$

$$= \frac{4 \times 10^{-5}}{R_{i}} \text{ watts/Hz}$$
 (2)

where R is the input resistance of the recorder. Therefore, the noise bandwidth of the tape recorder is given by

$$B_{n} = \frac{(69 \times 10^{-3})^{2} / R_{o}}{4 \times 10^{-5} / R_{i}}$$

$$= 119.0 \times \frac{R_i}{R_o} \text{ Hz}$$
 (3)

^{*}The upper frequency 100 kHz is sufficiently high compared to the practical frequency response of the tape recorder, so that this may be considered white noise.

2.3 Amplitude Response

The third test performed was a measurement of sinusoidal amplitude response. The results are plotted in Figure 4. The input level for this test was 1 volt, rms.

The frequency response was measured again after replacing the reproduce head with another unit. This was done to establish that the original unit was operating correctly. The results (also plotted in Figure 4) are similar enough to confirm that the original reproduce head was satisfactory.

3. PERFORMANCE CALCULATIONS

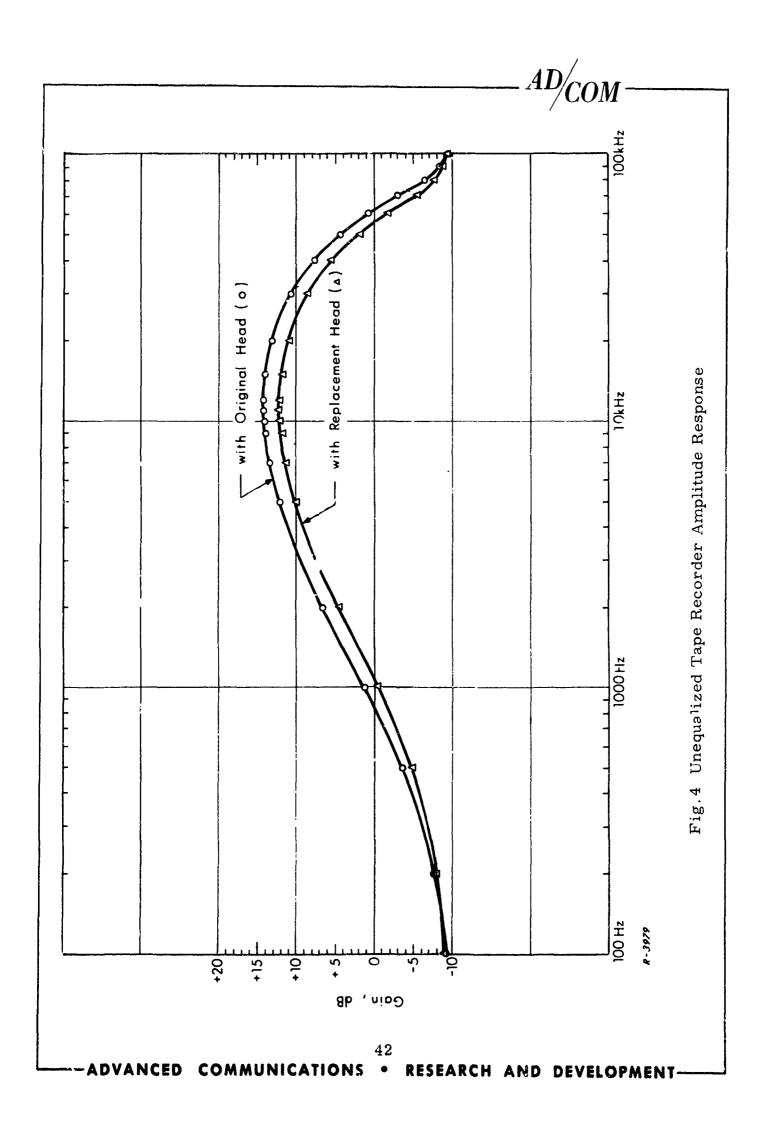
The purpose of this section is to obtain revised error performance predictions based on the measurements of Section 2. Reference to the data of Table 1 shows immediately that the basic error probability equation used in the earlier predictions is not applicable in this case. This equation (Equation 11 of G-103-1) applies when the two interference voltages (I_1 and I_2 of Table 1) are equal. The measurements indicate that these voltages are not equal. Therefore, we must obtain a more general error probability equation.

When each pulse interferes unequally with the preceding and succeeding pulses, the resulting signal amplitude at the sampling instant may have any of the four values $(S + I_1 + I_2)$, $(S + I_1 - I_2)$, $(S - I_1 + I_2)$ or $(S - I_1 - I_2)$, depending on the polarities of the adjacent pulses (and assuming the pulse being sampled causes the positive voltage S). The error probabilities corresponding to these cases will be

$$1 - \Phi\left(\frac{S + I_1 + I_2}{\sigma}\right),$$

$$1 - \Phi\left(\frac{S + I_1 - I_2}{\sigma}\right),$$

etc.





where $\Phi(x)$ is the gaussian distribution function defined by

$$\Phi(x) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{x} e^{-y^2/2} dy$$
 (4)

If the data is random and uncorrelated from bit-to-bit, each of the four cases occurs with probability one-fourth, so we may write the complete error probability as

$$P_{e} = \frac{1}{4} \left[i - \Phi \left(\frac{S + I_{1} + I_{2}}{\sigma} \right) + 1 - \Phi \left(\frac{S + I_{1} - I_{2}}{\sigma} \right) + 1 - \Phi \left(\frac{S - I_{1} + I_{2}}{\sigma} \right) + 1 - \Phi \left(\frac{S - I_{1} - I_{2}}{\sigma} \right) \right]$$

$$= 1 - \frac{1}{4} \left[\Phi \left(\frac{S + I_{1} + I_{2}}{\sigma} \right) + \Phi \left(\frac{S + I_{1} - I_{2}}{\sigma} \right) + \Phi \left(\frac{S - I_{1} + I_{2}}{\sigma} \right) + \Phi \left(\frac{S - I_{1} - I_{2}}{\sigma} \right) \right]_{(5)}$$

At each of the bit rates tested, I_1/S and I_2/S can be obtained from Table 1, so that Equation (4) can be plotted as a function of the remaining variable S/J in Figure 5.

The ideal case when $I_1 = I_2 = 0$ is also plotted in Figure 5. Comparison with the other curves indicates the degradation in performance due to intersymbol interference alone. For bit rates up to 50 kb/s, this degradation is less than 2 dB. At 62.5 kb/s, it is approximately 4 dB.

The curves of Figure 5 are plotted in terms of the output parameters S and σ . They do not contain any information as to whether the value of S/σ at the output of the tape recorder is comparable to the optimum value which would be produced by a matched filter. To include this information and to facilitate comparison with other performance results, these curves must be redrawn in terms of the input parameters E (signal energy per bit) and N_0 (input noise density). This conversion is explained pelow.

The rms noise output σ is related to input noise density N and the noise bandwidth B by Equation (1). The noise bandwidth was determined experimentally (see Section 2.2) and is

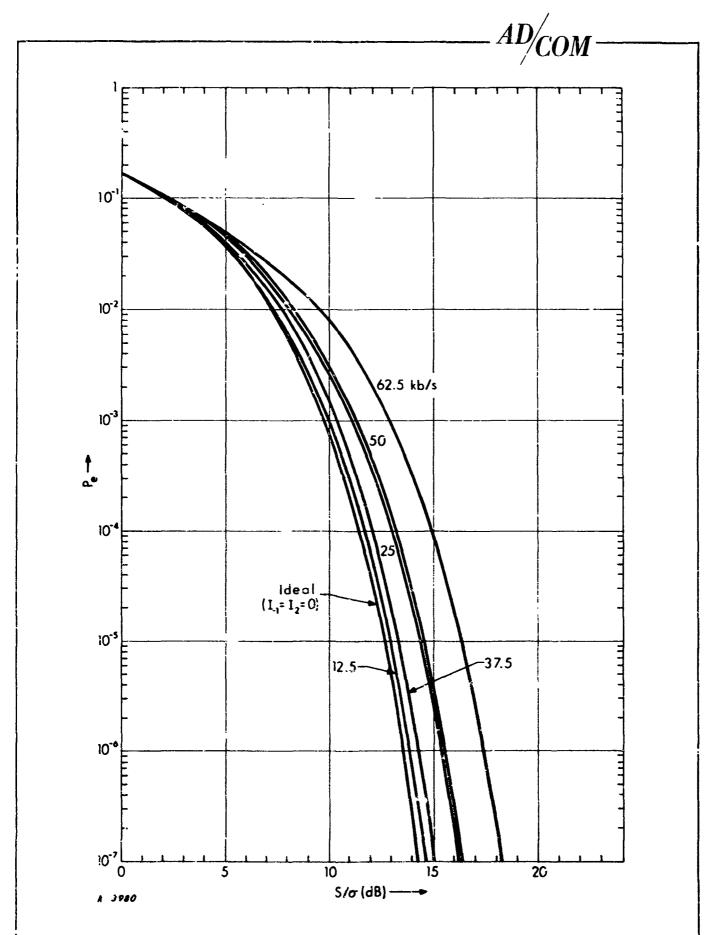


Fig. 5 Error Probability as a Function of S/σ for Various Data Rates at 15 ips

119.0
$$\times \frac{R_i}{R_o}$$
 Hz

Inserting this into Equation (1) we find that

$$\sigma = 10.91 \sqrt{R_i} \sqrt{N_o}$$
 (6)

Since the tape recorder is operating in its linear region, the peak output signal level S will be proportional to the peak input signal level, as long as the input waveshape is constant. In the present terminology, the input signal level is given by $\sqrt{\mathrm{ER_i/T}}$. Therefore, it is possible to determine a proportionality constant between S and $\sqrt{\mathrm{ER_i/T}}$. However, because pulse width varies with bit rate, this constant is different for each bit rate. Therefore, it must be calculated separately for each of the bit rates used in the experiments. The relevant data are summarized in Table 2. The peak signal level S was determined experimentally (see Section 2.1), the input signal level was held constant at 1.6 volts (peak). The ratio in the fourth column is obtained directly by division. This ratio holds for all input levels, although it was obtained from a single experimental measurement.

Table 2 COMPUTATIONS FOR CONVERTING TO E/N_{O}

	Experimental Values		Derived Relations	
1/T kb/s	S mv	$\sqrt{\frac{\text{ER}_{i}/\text{T}}{\text{volts}}}$	$S/\sqrt{ER_i/T}$	$\frac{S}{\sigma} / \sqrt{E/N_o}$ (dB)
12.5	104	1.6	6.50×10^{-2}	-3.57
25	80	1.6	5.00×10^{-2}	-2, 81
37.5	64	1.6	4.00 × 10 ⁻²	-3.00
50	44	1.6	2.75 × 10 ⁻²	-5.01
62.5	33	1.6	2.06 × 10 ⁻²	6,53



Now it is possible to combine the entries of the fourth column of Table 2 and Equation (6) to obtain the desired scale conversion. As an example, consider a bit rate of 12.5 kb/s, corresponding to the first line of Table 2.

The entry in column four may be rewritten as

$$S = 6.50 \times 10^{-2} \sqrt{ER_i/T}$$
 (7)

The value of T is $(12.5 \times 10^3)^{-1}$; inserting this gives

$$S = 7.24 \sqrt{ER_i}$$
 (8)

Dividing this result by Equation (6) we have

$$\frac{S}{\sigma} = 0.663 \sqrt{E/N_o}$$
 (9)

or, in decibels

$$20 \log_{10} \left(\frac{S}{\sigma} \right) = 10 \log_{10} (E/N_0) - 3.57 dB$$
 (10)

This is the result which appears in column five, line one of Table 2. The other entries in column five have been obtained in exactly the same way. These entries indicate how many dB's each of the curves of Figure 5 must be shifted (to the right) to convert the axis from S/σ to E/N_o . The result of this process is the set of performance curves shown in Figure 6.

An optimum matched filter produces a signal-to-noise ratio $\left(\frac{S}{\sigma}\right)$ at its output given by

$$\sqrt{\frac{2E}{N_o}}$$

That is, for matched filter processing

$$20 \log_{10} \left(\frac{S}{\sigma} \right) = 10 \log_{10} (E/N_0) + 3 dB$$
 (11)

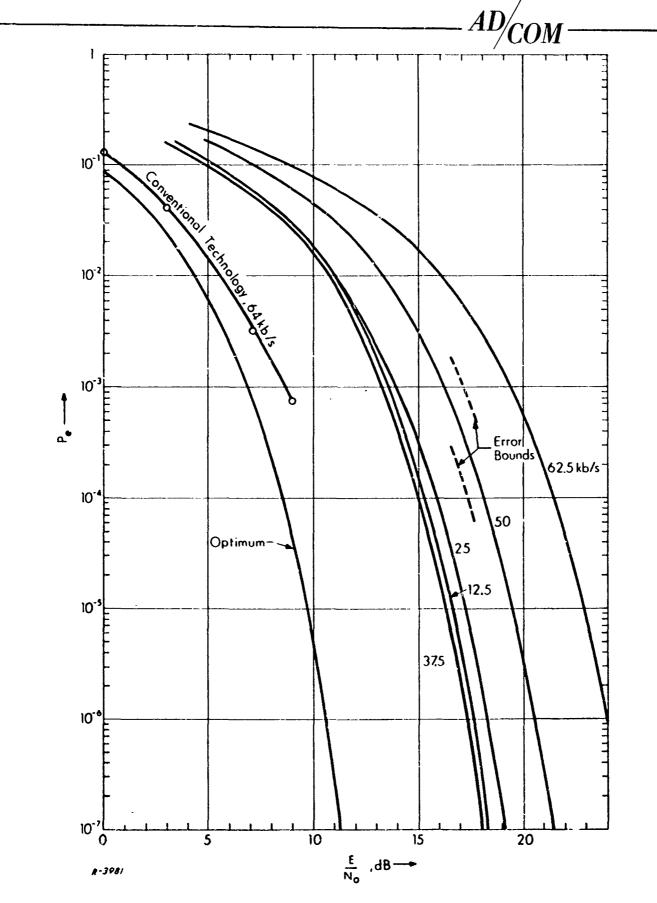


Fig : Error Performance of Proposed Scheme, Compared with Conventional Recording.

Therefore, the curve for optimum detection is plotted in Figure 6 by shifting the ideal curve from Figure 5 to the left by 3 dB.

One additional curve appears on Figure 6. It shows actual laboratory measurements of error probability obtained by GSFC personnel using the conventional recording method and a production signal conditioner.

4. DISCUSSION AND CONCLUSIONS

The curves of Figure 6 depict the overall performance degradation of the unconventional recording/reproduction technique from optimum. This degradation can be interpreted as the accumulation of two effects:

- a) Degradation due to intersymbol interference, and
- b) Degradation due to mismatch, i.e., reduced signal amplitude S at the sampling instant, compared to that obtained from an ideal matched filter.

The degradation due to intersymbol interference is shown quantitatively in Figure 5, and is less than 2 dB for bit rates up to 50 kb/s. At 62.5 kb/s, it is approximately 4 dB.

The degradation due to mismatch can be obtained from column five of Table 2, as follows. If there were no mismatch degradation, each curve of Figure 5 would be shifted (according to Eq. (11)) to the left by 3 dB to yield the curves in Figure 6. However, only the optimum curve was shifted to the left by this amount. The other curves were shifted to the <u>right</u> by the amounts indicated in column five of Table 2. Thus, the amount of this shift, plus 3 dB, is the degradation due to mismatch only. For instance, at 62.5 kb/s, the degradation due to mismatch is 9.53 dB. We conclude that mismatch caused significantly more degradation than intersymbol interference.

Before final conclusions as to the merits of the unconventional recording/reproduction scheme are drawn, certain limitations of the preceding results should be noted.

The first limitation is the experimental inaccuracy of ± 2 mv in the voltage measurements of the tape recorder pulse response. The measurements most sensitive to a 2 mv error are those of I_1 and I_2 , rather than S (see Table 1). Take the results for 50 kb/s as an example. The error performance for one point on this curve has been recalculated, assuming first that $\mathbf{I_1}$ and $\bf I_2$ are 2 mv greater than the measured values, second that $\bf I_1$ and $\bf I_2$ are 2 mv less than the measured values. The results are shown as dashed segments on Figure 6. They form bounds on the error introduced by the estimated experimental uncertainty. In terms of E/N, this error amounts to about ± 1 dB.

A second limitation to be kept in mind regarding Figure 6 is that the performance curves for the unconventional scheme are calculated from pulse measurements, rather than being actual measurements of error probability, as is the curve for existing technology. The comparison between the two would be somewhat more conclusive if both results represented actual measurement of error probabilit since this would eliminate all assumptions of interference mechanisms and noise statistics.

Finally, the performance calculations for the unconventional scheme have assumed perfect bit synchronization. In practice synchronization will not be perfect, resulting in some degradation in performance. The error probability measurements for conventional technology shown in Figure 6 include this degradation.

In spite of the forgoing reservations, Figure 6 indicates that performance of the unconventional scheme will be inferior to the performance measured by GSFC personnel with conventional technology. Comparison should be made for (approximately) equal bit rates; the predicted performance at 62.5 kbits/sec is 10 or 11 dB inferior to measured conventional performance at 64 kbits/sec. The are due to experimental inaccuracies or due to modelling difficulties and substantially alter this conclusion.